3705

MOS MONOLITHIC 8 CHANNEL MULTIPLEX SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3705 is an eight-channel multiplex switch with output enable control and one-out-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement Mode MOS technology. The logic input lines of the 3705 are NPN bipolar compatible and can be used directly with CCSL 5.0 volt logic levels with no level-shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

FEATURES

- **CCSL COMPATIBLE INPUT LOGIC LEVELS**
- **ONE-OUT-OF-EIGHT DECODER ON THE CHIP**
- **HIGH ON/OFF RATIO**
- **OUTPUT ENABLE CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

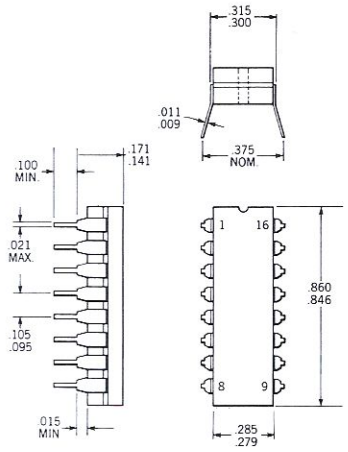
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any pin	+0.3 V
Negative Voltage on digital and analog input pins	−35 V
Negative Voltage on digital and analog output pins	−35 V
Negative Voltage on V_{DD} pin	−35 V
Total power dissipation in package ($T_A = 25°C$)	200 mW

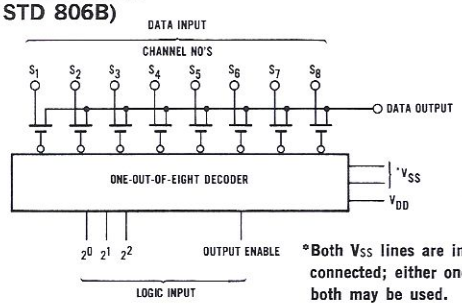
ORDERING INFORMATION — The 3705 is available for use in two signal ranges

−5.0 to +5.0 volts signal applications, Order A6J3705142
0 to +5.0 volts signal applications, Order A6J3705143

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



SYMBOLIC DIAGRAM
(MIL STD 806B)

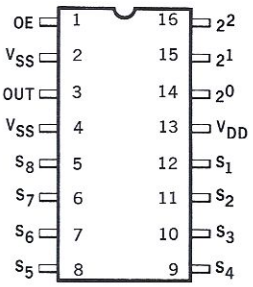


***Both V_{SS} lines are internally connected; either one or both may be used.**

TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

PIN CONFIGURATION
(16 lead DIP)



TOP VIEW

NOTES:

(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS

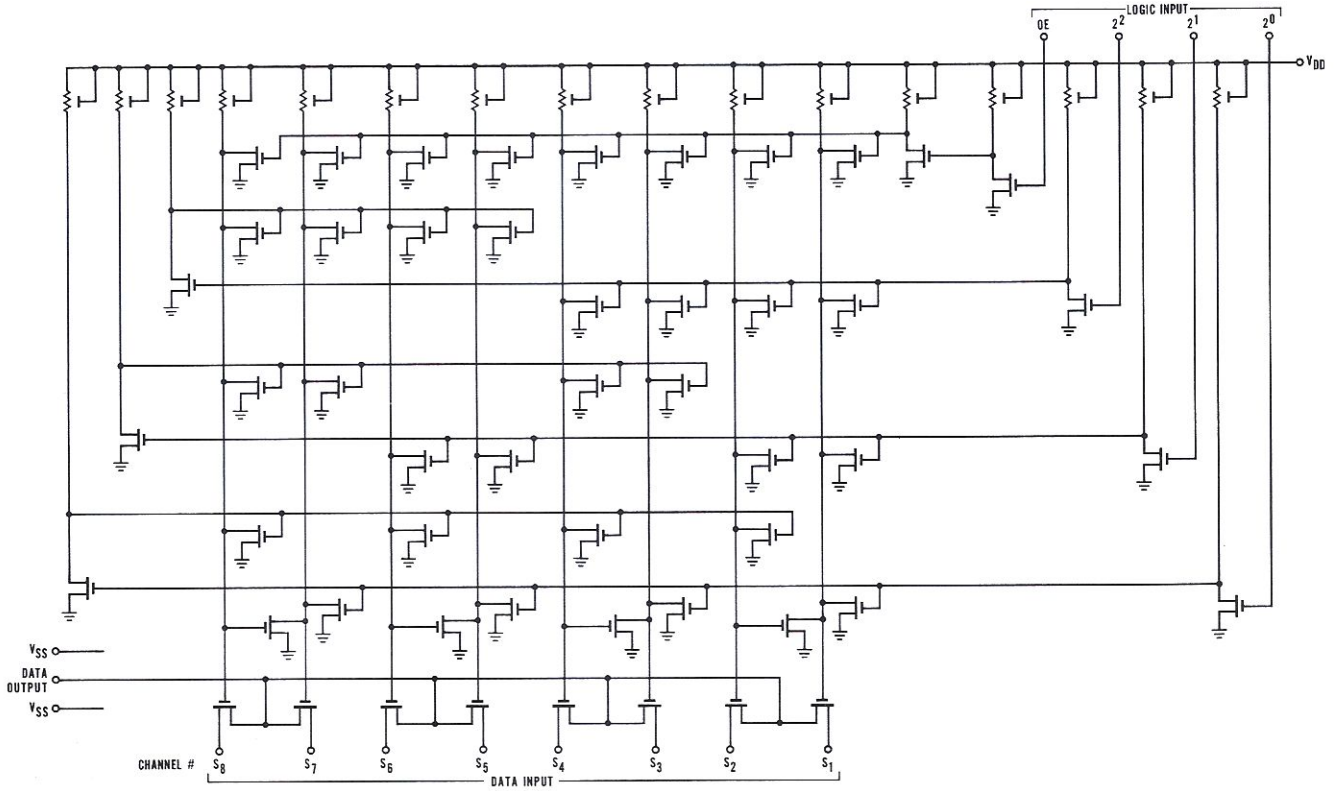
For 3705142: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

For 3705143: $0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance					
	142		250	400	Ω	$V_{OUT} = -5.0\ V$, $I_{OUT} = -100\ \mu A$
	143		190	350	Ω	$V_{OUT} = 0\ V$, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5			GΩ	$V_{SS} - V_{OUT} = 15\ V$
I_{LO}	Output Leakage Current			10	nA	$V_{SS} - V_{OUT} = 15\ V$
$I_{LO}(85°C)$	Output Leakage Current			500	nA	$V_{SS} - V_{OUT} = 15\ V$
I_{LDI}	Data Input Leakage Current					
	142			3.0	nA	$V_{SS} - V_{IN} = 15\ V$
	143			2.0	nA	$V_{SS} - V_{IN} = 10\ V$
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS} - V_{LOGIC\text{-}IN} = 15\ V$
*V_{IL}	Logic Gate Input "Low" Level	V_{DD}		+0.2	V	
*V_{IH}	Logic Gate Input "High" Level	$V_{SS} - 1.5$		V_{SS}	V	
t_S	Channel Switching Time (See Fig. 1)		1.0		μS	
C_{db}	Output Capacitance		40		pF	$V_{SS} - V_{OUT} = 0\ V$, $f = 1.0\ MHz$
C_{is}	Data Input Capacitance		7.5		pF	$V_{SS} - V_{IN} = 0\ V$, $f = 1.0\ MHz$
C_{ig}	Logic Input Capacitance		5.5		pF	$V_{SS} - V_{LOGIC\text{-}IN} = 0\ V$, $f = 1.0\ MHz$
P_D	Power Dissipation		130	175	mW	$V_{DD} = -31\ V$, $V_{SS} = 0\ V$

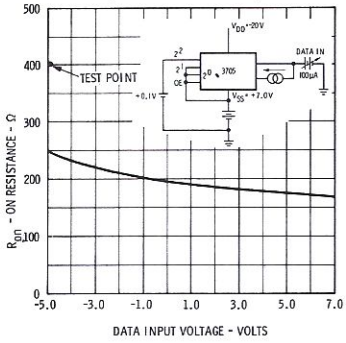
*When driven by CCSL elements, avoid excessive D.C. loading of CCSL elements to insure 3705 logic levels under maximum fan-out conditions.

SCHEMATIC DIAGRAM

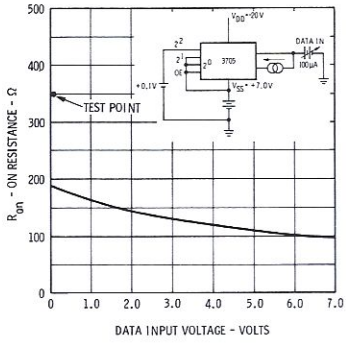


TYPICAL DEVICE CHARACTERISTICS

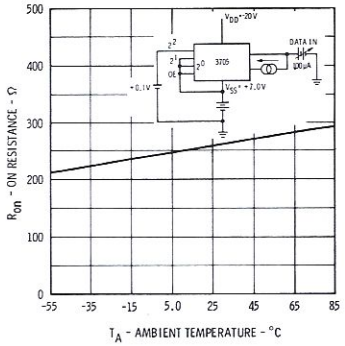
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 142 ONLY)



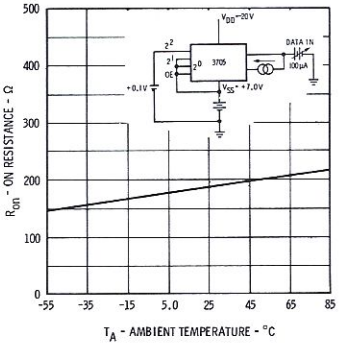
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 143 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 142 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 143 ONLY)



OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE

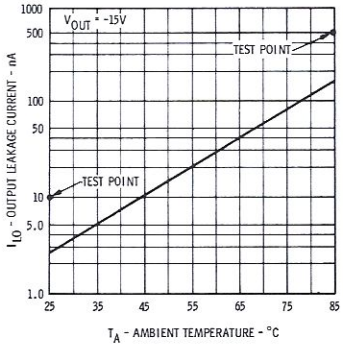
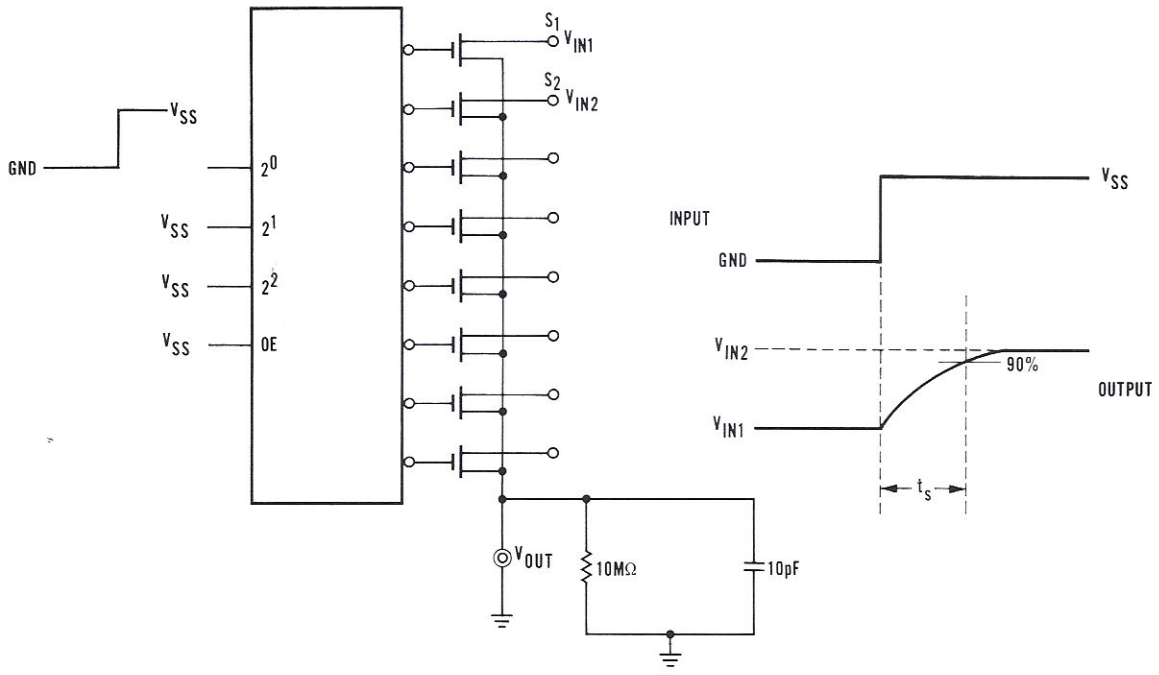
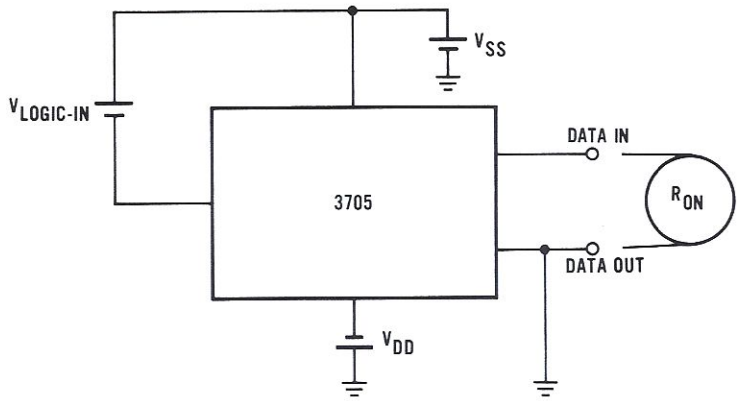


FIG. 1

SWITCHING TIME TEST CIRCUIT



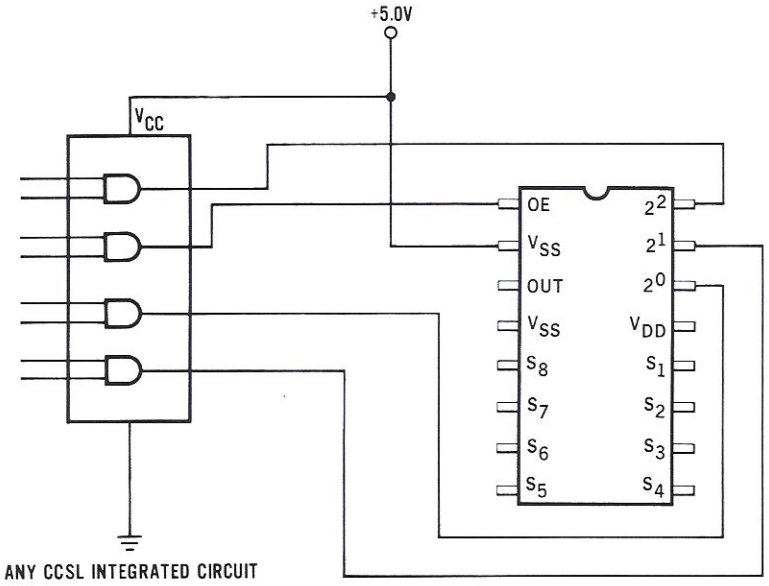


Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the 'ON' resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+7.0 V	+2.0 V
V_{DD}	−20 V	−25 V
LOGIC IN		
"Low" Level	+0.2 V	−4.8 V
"High" Level	+5.5 V	+0.5 V

TYPICAL CONTROL CIRCUIT



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